IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Bruce et al.	Examiner:	Mohamed, C.
Serial No.:	09/586,518	Group Art Unit:	2857
Filed:	June 2, 2000	Docket No.:	AMDA.455PA
Title:	Resistivity analysis		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service **in triplicate**, as first class mail, in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on July 17, 2003.

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APPEAL BRIEF

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Sir:

This is an Appeal Brief submitted pursuant to 37 CFR §1.192 for the above-referenced patent application and is being filed in triplicate.

I. Real Party in Interest

The real party in interest is Advanced Micro Devices, Inc. (AMD), of Sunnyvale, CA. The above-referenced patent application is assigned to AMD.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 4, 5 and 17 are allowed. Claims 1-3, 6-16 and 18-23 are presented for Appeal. Claims 1-3, 6-16 and 18-23 stand rejected under §102(e) as being anticipated by *Nikawa* (U.S. Pat. No. 6,160,407); claim 9 stands rejected under § 103(a) as being unpatentable over *Nikawa* in view of *Yue et al.* (U.S. Pat. No. 5,504,017); and claims 10, 22 and 23 stand rejected under §103(a) as being unpatentable over *Nikawa* in view of *Paniccia*

et al. (U.S. Pat. No. 5,872,360). The claims presented for appeal, as presently amended, may be found in the attached Appendix of Appealed Claims. Allowed claims 4, 5 and 17 are also reproduced in the Appendix for reference purposes.

IV. Status of Amendments

The application was initially filed on June 2, 2000, including claims 1-23. In reply to a first Office Action mailed on June 10, 2002, an Office Action Response was filed on September 10, 2002. An Office Action was mailed on November 18, 2002, and in reply, an Office Action Response and Amendment was filed on February 7, 2003, in which claims 1, 4 and 21 were amended. A Final Office Action was mailed on May 6, 2003. A Notice of Appeal was filed on July 2, 2003.

V. Summary of Invention

Appellant's invention is directed to resistive analysis of circuits. In one example embodiment, a semiconductor die having a resistive electrical connection is analyzed. Heat is directed to the die as the die is undergoing a state-changing operation that causes a failure due to suspect circuitry. The die is monitored, and a circuit path that electrically changes in response to the heat is detected and used to detect that a particular portion therein of the circuit is resistive. In this manner, the detection and localization of a semiconductor die defect that includes a resistive portion of a circuit path is enhanced.

In another example embodiment of the present invention, a semiconductor die is analyzed by heating at least a selected portion of state-changing circuitry in the die to cause a failure due to suspect circuitry at a suspect signal path site. The die is electrically operated in a loop that causes the die to fail at a selected failure rate, with the state-changing circuitry changing state in response to at least one of: an input frequency, a controlled voltage supplied to the die and a controlled die temperature. In response to the selected portion being heated, the state-changing transition between a failed mode and a recovered mode in the suspect signal path site is detected. The detected state-changing transition is used to determine that the signal path site has a resistivity that changes between the failed mode and the recovered mode.

VI. Issues for Review

Issue 1: Is the §102(e) rejection of claims 1-3, 6-16 and 18-23 proper when the cited reference fails to completely correspond to all of the claimed limitations?

Issue 2: Is the §102(e) rejection of claims 1-3, 6-16 and 18-23 proper when the Examiner improperly relied on an inherency-type argument in support of the Section rejection?

Issue 3: Are the §103(a) rejections of claims 9 and 10 proper when the Examiner failed to present teaching of elements that completely correspond to the claimed limitations?

Issue 4: Are the §103(a) rejections of claims 9, 10 and 22-23 proper when the Examiner failed to cite any evidence of motivation in support of the asserted modification of the primary '407 reference?

Issue 5: Is the §103(a) rejection of claims 10 and 22-23 proper when the asserted modification of the primary '407 reference would render the reference unsatisfactory for its intended purpose?

Issue 6: Can the Section 103(a) rejections be maintained when the Examiner failed to answer the substance of the Appellant's traversal as required by M.P.E.P.§707.07(f)?

VII. Grouping of Claims

The claims as now presented do not stand and fall together and are separately patentable for the reasons discussed in the Argument. Claim 1 is in group 1; claims 2, 6 and 11-16 are in group 2, claim 3 is in group 3, claims 7 and 8 are in group 4, claim 9 is in group 5, claim 10 is in group 6, claim 18 is in group 7, claims 19-20 are in group 8 and claims 22-23 are in group 9.

VIII. Argument

Appellant submits that the claims of groups 1-9 are patentably distinguishable from each other and from the cited prior art references. Claim 1 in group 1 is patentable over the prior art because it includes subject matter that is not taught or suggested by any of the

references cited including identifying a circuit path that electrically changes while using a state-changing operation of suspect circuitry including the circuit path. The claims in group 2 are separately patentable over the other claim groups because they are directed to subject matter that includes detecting a state-changing transition between a failed mode and a recovered mode, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claim 3 in group 3 is separately patentable over the other claim groups because it is directed to subject matter that includes operating a die to cause circuitry to change state in response to various controls, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claims 7 and 8 in group 4 are separately patentable over the other claim groups because they are directed to subject matter that includes determining a location of a resistive signal path site, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claim 9 in group 5 is separately patentable over the other claim groups because it is directed to subject matter that includes detecting a change in failure rate of a circuit path, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claim 10 in group 6 is separately patentable over the other claim groups because it is directed to subject matter that includes thinning a die prior to heating, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claim 18 in group 7 is separately patentable over the other claim groups because it is directed to subject matter that includes a system having means for detecting a state-changing transition between a failed mode and a recovered mode and means for using the detected state-changing transition, determining that a signal path has a resistivity, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claims 19-20 in group 8 are separately patentable over the other claim groups because they are directed to subject matter that includes a detector adapted to detect a state-changing transition and a display adapted to use the detected state-changing transition for determining a signal path site that has a resistivity, which would not necessarily be present in the other claim groups and is not taught by the cited prior art. Claims 22-23 in group 9 are separately patentable over the other claim groups because they are directed to subject matter that includes a photodetector and position sensor, which would not necessarily be present in the other claim groups and is not taught by the cited prior art.

Issue 1: The §102(e) rejection of claims 1-3, 6-16 and 18-23 is improper because the cited reference fails to show elements that completely correspond to all of the claimed limitations.

The Section 102(e) rejection in connection with all of the claim groups must be reversed because the Examiner failed to show complete correspondence between the cited portions of the '407 reference and the limitations in the rejected claims. Specifically regarding the rejections of the independent claims, the asserted interpretation of the '407 reference is erroneous because the change in resistivity (asserted as a "state-changing" operation) does not teach a state-changing operation as claimed. Applicant's invention includes limitations directed to identifying the specific circuit paths that electrically change in response to heat and detecting that a particular circuit portion therein is resistive -- using a state-changing operation of a suspect circuit to cause its failure. The '407 reference does not teach these limitations because it does not use a state-changing operation of a suspect circuit to cause its failure. Rather, the alleged "state-changing" operation is the change in resistance of a circuit caused by local heating, and the change in resistance itself is what is detected.

For example, claim 1 (group 1) is directed to subject matter directed to identifying a circuit path that electrically changes while using a state-changing operation of suspect circuitry. The citations at page 2 of the Final Office Action, referring to columns 4 and 8 of the '407 reference, are merely directed to "local heating of the wiring" (Col. 4, lines 15-16) for the purpose of determining a potential flaw somewhere in the integrated circuit. The Examiner has not asserted, nor can the Appellant find, anywhere in the '407 reference where a circuit path is identified *while* using a state-changing operation of suspect circuitry. In addition, the local heating referred to in the '407 reference does not involve state-changing operations of such suspect wiring in the context of claim 1 or the other independent claims, as alluded to above. For instance, the Examiner's assertion on page 6 of the Final Office Action that a "state-changing operation of a suspect circuit is the current variation" is unsupported and fails to teach a state-changing operation in the context of the claimed invention (*e.g.*, logical state-changing). Specifically, while the Examiner asserts that heating a wire would expand the wire, the Examiner has not showed how this alleged "state-changing" operation causes a failure. It appears that the Examiner is confusing the state-changing operation with the electrically-changing circuit path; specifically, the expanding

wire referred to as the state-changing operation is instead the suspect circuit itself (*i.e.*, the wire not being perfectly connected). Furthermore, the Examiner's inherency-type argument on page 6 of the Final Action, in addition to being improper as discussed in Issue 2 below, fails to teach the claimed limitations directed to using a state-changing operation to cause a failure. Therefore, the elements cited on page 6 of the Final Office Action do not teach the state-changing and identification limitations as claimed.

The Examiner's citations to columns 15 and 16 of the '407 reference are also improperly asserted as teaching of the limitations directed to "state-changing" operations. The cited portions describe a defective IC detection approach in which OBIRCH signals are used to make a judgment whether the IC's current drain value is unusual or not. *See* Col. 16, lines 51-53. The '407 reference specifically teaches that an area as wide as possible should be scanned to make the detection of a failure easier. *See* Col. 16, lines 20-25. Thus, the rejection relying on these cited portions of the '407 reference is also flawed because state-changing operations of the suspect circuit are not used to detect a particular circuit portion therein that is resistive. Rather, the '407 reference employs the visible laser generating beam section 51 and the microscope section 52 to further localize a defective wiring portion. *See* Col. 15, lines 58-61.

Further in regard to the Section 102(e) rejection, various other ones of the claimed limitations are not shown in the cited reference, and in some instances, ignored entirely by the Examiner. For example, claim 3 (group 3) is directed to subject matter including "electrically operating the die to cause the circuitry to change state in response to at least one of: an input frequency, a controlled voltage supplied to the die and a controlled die temperature." The Examiner asserted no teaching whatsoever of these limitations. Regarding claims 7 and 8 (group 4), the Examiner has not asserted any teaching of limitations directed to identifying or determining a location of a resistive signal path site. Regarding claim 9 (group 5), as the Examiner acknowledges on page 4 of the Final Office Action, the '407 reference fails to teach limitations directed to "detecting a change in a failure rate of the circuit path during a state-changing operation." Regarding claim 10 (group 6), the Examiner acknowledges on page 4 of the Final Office Action that the '407 reference fails to teach "thinning the die prior to the heating." Regarding claim 11 (group 2), the Examiner has not cited any reference showing the limitation directed to heating state-

changing circuitry and causing a suspect signal path site to expand. No reference has been cited as teaching the limitations in claim 14 (group 2) directed to observing a delayed response from a die. Regarding claims 19-23 (groups 8 and 9), the Examiner has not shown any teaching for limitations directed to a detector adapted to detect a state-changing transition. Specifically regarding claims 22-23 (group 9), the Examiner acknowledged on page 4 of the Final Office Action that the '407 reference fails to teach or suggest a photodetector as claimed. The above instances are merely examples of the various claimed limitations that the Examiner completely ignored; additional limitations were similarly not addressed.

In view of the above, the Examiner failed to meet the requirements that a Section 102(e) reference include elements that completely correspond to every claimed limitation; therefore, the Section102(e) rejection is improper and should be reversed.

Issue 2: The §102(e) rejection of claims 1-3, 6-16 and 18-23 is improper because the Examiner improperly relied on an inherency-type argument in support of the Section rejection.

The Section 102(e) rejection in connection with all of the claim groups must be reversed because the Examiner relied on an assertion of inherent features involving state-changing transitions between failed and recovered modes, without providing any supporting evidence. Clearly, a state-changing transition can occur (*e.g.,* to a failed state) without recovery. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 20 U.S.P.Q.2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). In this instance, the Examiner asserted that a state-changing transition between failed and recovered modes is inherent because an expanding wire, when heated, would conduct current (see page 6 of the Final Office Action). The Examiner's argument is illogical, because failed wires (like fuses) seldom expand sufficiently to reconnect and

thereby conduct current. Appellant submits that this alleged transition is not necessarily present and, without any supporting extrinsic evidence, fails the above-discussed test for establishing inherency. Therefore, the Section 102(e) rejection must be reversed.

Issue 3: The §103(a) rejections of claims 9 and 10 are improper because the Examiner failed to present teaching of elements that completely correspond to the claimed limitations.

The Section 103 rejections of claims 9 and 10 (groups 5 and 6) must be reversed because they fail to establish *prima facie* obviousness; the cited references fail to teach elements that completely correspond to all of the claimed limitations, including those directed to the detection of a failure rate of a circuit path. To establish a *prima facie* case of obviousness, three basic criteria must be met, as indicated in the M.P.E.P. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In this instance, the Office Action failed to meet all of the criteria for establishing such a Section 103(a) rejection. This Issue addresses the third criterion, with Issue 4 below discussing the first criterion requiring evidence of motivation. Issue 5 also addresses the first criterion in the context of the rejection of claims 10 and 22-23. The rejection of claim 9 must be reversed in view of either one of Issues 3 or 4, and the rejection of claim 10 must be reversed in view of any one of Issues 3, 4 or 5.

Specifically regarding the third criterion for establishing a *prima facie* Section 103 rejection, the Examiner failed to show elements corresponding to all of the claimed limitations as discussed above in connection with Issue 1, as applied to claims 9 and 10. In a hindsight attempt to combine references to arrive at the presently claimed invention, the Examiner further ignored the plain language of the limitations directed to failure rate. For instance, claim 9 is directed to a method of analyzing a semiconductor die including, *inter alia*, "detecting a change in a failure rate of the circuit path during a state-changing operation." Examiner acknowledged at page 4 of the Final Office Action that the '407 reference fails to teach these limitations. In an attempt to overcome this deficiency, the

Examiner erroneously referred to two portions of the '017 reference. The cited portions of the '017 reference are directed to a teaching that failure rates may be high, but neither portion teaches detecting a change in failure rate, as claimed. In view of the above discussion regarding the '407 reference's lack of correspondence to the claimed invention and the fact that the '017 reference fails to teach the asserted claim limitations, the Section 103(a) rejections of claims 9 and 10 must be reversed.

Issue 4: The §103(a) rejections of claims 9, 10 and 22-23 are improper because the Examiner failed to cite any evidence of motivation in support of the asserted modification of the primary '407 reference.

The Section 103(a) rejection of claims 9, 10 and 22-23 (groups 5, 6 and 9) must also be reversed because the Examiner failed to properly provide evidence from the prior art in support of modifying the primary '407 reference to arrive at the presently-claimed limitations. Instead of citing evidence of motivation, the Examiner conclusively asserted motivation in view of the Appellant's disclosure without citing any evidence in support therefor. As discussed above, establishing a *prima facie* case of obviousness requires suggestion or motivation for making the modification; relevant case law further requires that the suggestion or motivation be more than conclusory and, specifically, be supported by evidence in the prior art. *See, e.g., Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 U.S.P.Q.2d 1161 (Fed. Cir. 2000) ("Our court has provided [that the] motivation to combine may be found explicitly or implicitly: 1) in the *prior art references* themselves; 2) in the knowledge of those of ordinary skill in the art that certain *references*, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to *references* relating to possible solutions to that problem.'"). As applied here, the Examiner failed to cite any evidence showing that modifying the primary '407 reference to allegedly arrive at the limitations of the present invention would be motivated.

Specifically, no evidence has been provided to show any teaching or suggestion for using the '407 reference in connection with detecting a failure rate change, as claimed in the instant invention, or for modifying the reference to achieve other claimed limitations. For instance, the Examiner asserts on page 4 of the Final Office Action that one of skill in the art

would be motivated to modify the '407 reference "because the detection of change in failure rate during a state-changing operation would determine if the failure rate increase[s] or decreases during that state-changing operation an[d] therefore would indicate defects in the die." This quotation cites no evidence from the prior art for determining a change in failure rate and/or indicating defects in the die. It would appear that the Examiner has instead either speculated as to motivation or used the disclosure of Appellant's invention as a blueprint for piecing together the asserted references; relevant case law indicates that such a hindsight approach is improper. *See, e.g., In re Dembiczak* 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) ("Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight").

The other Section 103 claim rejections should similarly fail for the Examiner's failure to cite evidence of motivation for modifying the '407 reference. Regarding the rejection of claim 10 on page 4 of the Final Office Action, the Examiner asserted, without supporting evidence, that "tinning the die would increase the transmission of the laser beam into the die; therefore, the current varies as well as the resistivity which determine the presence of a failure in the die." In addition to failing to cite evidence in support of this assertion, the Examiner failed to show any evidence of motivation showing how thinning the die would affect the determination of the presence of failures in any die of the '407 reference, in the context of the disclosure therein. Regarding the rejection of claims 22 and 23 on pages 4 and 5 of the Final Office Action, the Examiner asserted, again without any supporting evidence, that one of skill in the art would be motivated to modify the '407 reference with the claimed limitations "because it would detect a change in the reflected light that leads to a change in voltage and current in the die and consequently a change of resistivity would be detected." Appellant submits that this statement by the Examiner, in addition to being without supporting evidence, also fails to address how one would be motivated to detect a change in reflected light in the context of the '407 reference.

Without recitation of evidence in support of the above-mentioned assertions, the Examiner's assertions are merely speculative, perhaps relying upon a hindsight reconstruction of the cited references in view of the Appellant's invention. The purpose of requiring evidence of motivation for modifying a reference is specifically intended to avoid

such an improper reconstruction in hindsight. *See, e.g., In re Dembiczak* 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999). Therefore, the Section 103(a) rejection must be reversed.

Issue 5: The §103(a) rejection of claims 10 and 22-23 is improper because the asserted modification of the primary '407 reference would render the reference unsatisfactory for its intended purpose.

The Section 103(a) rejection of claims 10 and 22-23 (groups 6 and 9) must be reversed because modifying the primary '407 reference as asserted by the Examiner would undermine its stated purpose of non-destructive analysis. Specifically, a proposed combination that undermines the operation and/or purpose of the main embodiment cannot be maintained. *See, e.g., In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines purpose of main reference.). In this instance, the Examiner's proposed combination is a modification of one of the '407 reference's objects and would clearly undermine its respective operation and purpose.

The analysis of circuit wiring to which the '407 reference is directed involves a "non-destructive" method that largely leaves the device being analyzed intact. *See* Col. 3, lines 53-59 and Col. 4, lines 34-38. The '407 reference teaches heating the die to determine whether a failure exists (*see, e.g.,* Figs. 21 and 23, S142-S147 and S152-S154 respectively), and the chip is only inspected using the visible-beam-microscope arrangement to determine where the failure occurs if a failure is detected. By first thinning the die, the die will be destroyed before it can be determined that the die is defective. This is directly contrary to the object of the '407 reference and directly contrary to the operation taught therein (*see e.g.*, Col. 18, lines 35-48). To allege under §103 that a skilled artisan would modify the '407 reference in such a manner is untenable and impermissible under §103, as discussed above.

Moreover, the Office Action asserts a combination of reference teachings that would undermine another important aspect taught by the '407 reference. The Office Action citations refer to the fifth embodiment of the '407 reference wherein the device under test (DUT) is never removed from the support structure of the testing/inspection system of Figure 20. *See* Figs. 20-21 and the discussion at col. 15-17 (*e.g.,* column 15, lines 60-62). In order

to thin the back side of the DUT, the DUT would have to be removed from the test/inspection system, thinned, and then placed back in the system. This modified process directly contradicts the '407 reference's teachings and advantages of the fifth embodiment. Such asserted modifications evidence that the prior art *teaches away* from the claimed invention; thus, there is no motivation for modifying the '407 reference and the Section 103(a) rejection must be reversed. *See, e.g., In re Gordon.*

Issue 6: The Section 103(a) rejections cannot be maintained because the Examiner failed to answer the substance of the Appellant's traversal as required by M.P.E.P.§707.07(f).

The Examiner failed to address the traversal of the asserted modifications of the '407 reference in connection with both Section 103(a) rejections as presented by the Appellant. M.P.E.P. 707.07(f) states, in pertinent part, the following:

> Where the requirements are traversed, or suspension thereof requested, the examiner should take proper reference thereto in his or her action on the amendment. Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it. If a rejection of record is to be applied to a new or amended claim, specific identification of that ground of rejection, as by citation of the paragraph in the former Office letter in which the rejection was originally stated, should be given.

In this regard, M.P.E.P. 707.07(f) indicates that the Office Action should take note of the Appellant's argument regarding the impropriety of the asserted combination and answer the substance of it. This is consistent with the purpose of aiding the Appellant in judging the propriety of continuing the prosecution, as indicated in 37 C.F.R. §1.104(a)(2). In this instance, the Examiner failed to even acknowledge the Appellant's traversal of the Section 103(a) rejections for lack of motivation (the first criterion discussed above in connection with Issue 2). By failing to comply with this requirement, the Examiner did not afford the Appellant the opportunity to judge the propriety of the §103(a) rejection and to form a response thereto. Therefore, in the event that all claims are not allowed, Appellant requests that the final rejections in the Final Office Action be reversed, that the Examiner take reference to the traversal and that the Appellant have an opportunity to respond thereto.

IX. Conclusion

In view of the above, Appellant believes the claimed invention to be patentable. Claims 1-23 remain for consideration. Appellant respectfully requests reversal of the rejection as applied to the appealed claims and allowance of the entire application.

Please charge Deposit Account number 01-0365 (TT3843) in the amount of $320.00 for filing a Brief in support of an appeal as set forth in §1.17(c).

Respectfully submitted,

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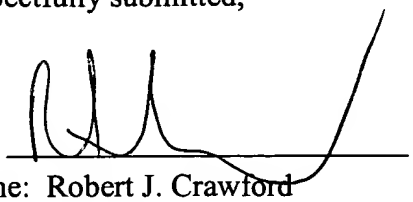
By: 
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APPENDIX OF APPEALED CLAIMS (09/586,518)

1. A method for analyzing a semiconductor die having suspect circuitry that includes a multitude of circuit paths, the method comprising:

while using a state-changing operation of the suspect circuitry to cause a failure due to the suspect circuitry, identifying one of the circuit paths that electrically changes in response to heat and detecting that a particular circuit portion therein is resistive.

2. A method for analyzing a semiconductor die, the method comprising:

heating at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal path site;

detecting, in response to the selected portion being heated, a state-changing transition between a failed mode and a recovered mode in the suspect signal path site; and

using the detected state-changing transition, determining that the signal path site has a resistivity that changes between the failed mode and the recovered mode.

3. The method of claim 2, further comprising electrically operating the die to cause the circuitry to change state in response to at least one of: an input frequency, a controlled voltage supplied to the die and a controlled die temperature.

4. A method for analyzing a semiconductor die, the method comprising:

heating at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal path site;

detecting, in response to the selected portion being heated, a state-changing transition between a failed mode and a recovered mode in the suspect signal path site;

using the detected state-changing transition, determining that the signal path site has a resistivity that changes between the failed mode and the recovered mode;

electrically operating the die to cause the circuitry to change state in response to at least one of: an input frequency, a controlled voltage supplied to the die and a controlled die temperature; and

electrically operating the die in a loop that causes the die to fail at a selected failure rate.

5. The method of claim 4, wherein detecting a state-changing transition includes detecting that the failure rate has changed.

6. The method of claim 2, wherein heating at least a selected portion of state-changing circuitry in the semiconductor die includes scanning the die with a laser.

7. The method of claim 6, further comprising:

identifying the portion of the die at which the laser is directed while detecting the state-changing transition, wherein determining that the signal path site has a resistivity that changes includes determining that the signal path site changes when scanned with the laser; and

using the identified portion to determine the location of the resistive signal path site.

8. The method of claim 2, wherein using the detected state-changing transition includes using an image of the operating circuitry and a map of signal paths, further comprising using the image and map to identify the location of the resistive signal path site.

9. The method of claim 2, wherein identifying one of the circuit paths that electrically changes in response to heat includes detecting a change in a failure rate of the circuit path during a state-changing operation.

10. The method of claim 2, further comprising thinning the die prior to the heating.

11. The method of claim 2, wherein heating at least a selected portion of state-changing circuitry includes causing the suspect signal path site to expand.

12. The method of claim 2, further comprising obtaining a cross-sectional image of the suspect signal path site and determining therefrom the portion of the signal path site having a resistivity that changes.

13. The method of claim 2, wherein detecting a state-changing transition between a failed mode and a recovered mode includes detecting that the die is operating improperly.

14. The method of claim 2, further comprising observing a delayed response from the die and determining therefrom that the die includes a resistive defect, prior to the heating.

15. The method of claim 2, further comprising using a scanning optical microscope (SOM).

16. The method of claim 2, further comprising placing the die in a test arrangement adapted to electrically operate the die under selected operating conditions and to obtain a response from the die including the state-changing transition.

17. A method for testing an integrated circuit (IC), the method comprising:

operating the IC in a loop that causes the IC to fail at a selected failure rate;

laser-scanning the IC and detecting a response from the IC, the response including a change in the failure rate of the IC responsive to laser scanning a portion of the IC;

using the detected response as an input control to a contrast amplifier of a display adapted to receive image data including reflected light data from the laser scanning of the IC;

displaying the image data using the contrast amplifier to control the contrast of the image; and

identifying the portion of the IC being scanned that corresponds to the change in failure rate as a portion of the image having a variation in contrast and detecting therefrom that the portion includes a resistive interconnect.

18. A system for analyzing a semiconductor die, the system comprising:

means for heating at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal path site;

means for detecting, in response to the selected portion being heated, a state-changing transition between a failed mode and a recovered mode in the suspect signal path site; and

means for using the detected state-changing transition, determining that the signal path site has a resistivity that changes between the failed mode and the recovered mode.

19. A system for analyzing a semiconductor die, the system comprising:

a scanning optical microscope (SOM) adapted to direct a laser and heat at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal path site;

a detector adapted to detect, in response to the selected portion being heated, a state-changing transition between a failed mode and a recovered mode in the suspect signal path site; and

a display adapted to use the detected state-changing transition and to display an image of the die to be used for determining that the signal path site has a resistivity that changes between the failed mode and the recovered mode.

20. The system of claim 19, wherein the SOM, the detector, and the display are communicatively coupled to each other.

21. The system of claim 20, wherein the display includes an image contrast amplifier, and wherein the detector includes an output adapted to supply a control signal to the image contrast amplifier in response to the transition between the failed mode and the recovered mode.

22. The system of claim 21, wherein the SOM further comprises:

a photodetector adapted to detect reflected light from the die as it is scanned with the laser and to provide a signal representing the detected light to the display; and

a position sensor adapted to provide the position of the laser upon the die.

23. The system of claim 22, wherein the display is adapted to use the signal representing the detected light and the position sensor to display an image of the die, and wherein the contrast of the image of the resistive signal path is altered from that of a non-defective die.